REMARKS

Claims 1 and 6-13 are presented for consideration, with Claim 1 being independent.

Independent Claim 1 has been amended to further distinguish Applicants' invention from the cited art.

Initially, Claims 1 and 6-13 stand rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement. This rejection is based on the allegation that the claimed "effective voltage calculating circuit" and "compensation value calculating circuit" are not adequately supported in the specification.

In response to this rejection, the Examiner's attention is respectfully directed to Figure 1 and page 29, last paragraph, for support of Applicants' claimed effective voltage calculating circuit for finding an effective voltage value on the basis of image data (Din[I]). Additionally, support for Applicants' claimed compensation value calculating circuit can be found, for example, in Figure 1 and the specification beginning on page 30, line 10, in which a voltage drop quantity is determined. Accordingly, it is submitted that all elements of Applicants' claimed invention are adequately supported in the specification, and therefore reconsideration and withdrawal of the rejection of Claims 1 and 6-13 under 35 U.S.C. §112, first paragraph, is respectfully requested.

Claims 1 and 6-13 also stand rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement. This rejection is directed to

Applicants' claimed "effective voltage calculation circuit." It is submitted that the same portions of the specification and drawings discussed above regarding support for this feature can also be relied on to enable one of ordinary skill in the art to find an effective voltage value based on image data. Accordingly, reconsideration and withdrawal of the rejection of Claims 1 and 6-13 under 35 U.S.C. §112, first paragraph, is respectfully requested.

Claims 1 and 6-13 are rejected under 35 U.S.C. §103 as allegedly being obvious over Suzuki '361 in view of Sarrasin '000. This rejection is respectfully traversed.

Claim 1 of Applicants' invention relates to an image display apparatus comprised of electron-emitting devices driven in a matrix by a plurality of row wirings and column wirings, a scanning circuit for sequentially selecting and scanning the row wirings, and a modulation circuit for applying a modulated signal to the column wirings. In addition, a voltage drop compensation circuit calculates corrected image data for reducing an influence of voltage drops due to at least resistance components of the row wirings, with respect to image data. As amended, the modulation circuit generates a modulated signal by modulating both a pulse width and a voltage amplitude, and an effective voltage calculating circuit finds an effective voltage value on the basis of the image data, with the effective voltage value being a value obtained by averaging in a time direction a voltage amplitude value of a modulated signal corresponding to the image data for one horizontal scanning period. Still further, a compensation value calculating circuit calculates a compensation value for reducing an influence of voltage drops due to at least

resistance components of the row wirings, with respect to the effective voltage value, and the modulation circuit outputs a modulated signal on the basis of the corrected image data.

In accordance with Applicants' claimed invention, a high performance image display apparatus is provided.

The primary citation to Suzuki relates to an electron beam generating device and is said to include all of the features of Applicants' Claim 1, with the exception of a modulation circuit for applying a modulated signal having a voltage amplitude which varies in one pulse signal. More specifically, Suzuki shows an image display that includes a scanning circuit 202 and a modulating signal generator 209 for driving a display panel 201. Suzuki is also said to include a voltage drop compensation circuit, a compensation value calculating circuit and an effective voltage calculating circuit as set forth in Applicants' Claim 1.

The secondary citation to Sarrasin relates to a display device and is relied on for its teaching of providing a modulated signal having an amplitude which varies in one pulse signal.

It is respectfully submitted, however, that the proposed combination of Suzuki and Sarrasin, even if proper, still fails to teach or suggest Applicants' claimed invention. For example, Claim 1 now sets forth an effective voltage calculating circuit that finds an effective voltage value on the basis of the image data, with the effective voltage value being a value obtained by averaging in a time direction a voltage amplitude value of a modulating signal corresponding to the image data for one horizontal scanning period. Support for this claim

feature can be found, for example, on page 29, lines 12-27 of the specification. In Suzuki, on the other hand, a memory 207, which the Office Action analogizes to Applicants' claimed effective voltage calculating circuit, stores correction rates based on row by row luminance.

Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. §103 is respectfully requested.

Therefore, it is submitted that Applicants' invention as set forth in independent Claim 1 is patentable over the cited art. In addition, dependent Claims 6-13 set forth additional features of Applicants' invention. Independent consideration of the dependent claims is respectfully requested.

SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

In compliance with the duty of disclosure under 37 C.F.R. § 1.56 and in accordance with the practice under 37 C.F.R. §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed Form PTO-1449. Copies of the listed documents are also enclosed.

The concise explanations of relevance for the non-English documents are provided by their accompanying English-language abstracts.

For the Examiner's additional information, U.S. Patents No. 5,734,361 and No. 6,580,407 correspond to Japanese Document No. 8-248921.

These documents were cited in a Japanese Office Action dated August 21, 2007, in a corresponding Japanese patent application. In the Japanese Office Action, the Examiner made the following comments:

Japanese Document No. 08-248021 discloses an electron-emitting display apparatus which modulates pulse amplitude for reducing an influence of voltage drops due to at least resistance components of row wirings.

A gradation control by a combination of a pulse amplitude modulation and a pulse width modulation is well-known art as shown in Japanese Documents No. 2001-109421 and No. 2002-311885. It is perceived that a person skilled in the art could have easily applied this technique to Japanese Document No. 08-248921.

Gain adjusting to fall a value of gradation-corrected data within a dynamic range is well-known as shown in Japanese Document No. 10-207424 and PCT Document No. WO 97/33271.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be returned indicating that such information has been considered.

CONCLUSION

Due consideration and prompt passage to issue are respectfully requested.

Applicants' undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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